November 17, 2004 Barrel Electronics VC Minutes

Agenda items:
-Status of designs
-Plans for testing AR2B
-Low voltage offset studies in the test-beam.
-Miscellaneous items

Inter-meeting issues:

Daniel inquired about the status of chip testing at PENN. Penn is concentrating on DTMROC testing (or rather re-testing) at the moment in order to get statistics on how many extra wafers will need to be packaged. They are finding a fair amount of good chips that were failed the first time through. It is looking like somewhere between 3 and 7 extra wafers of DTMROCs will need to be packaged.

As for the ASDBLRs, PENN has been testing for more test pulse capacitor failures. The test has just been expanded to check the A and B inputs. The B inputs should be protected from outside harm, and so if this is happening because of some outside stimulus, they expect to see no (or many fewer) TP capacitor failures on the B inputs. At the time of the meeting, this new test had just started and no results were available.

NBI reported that the current lot of barrel boards in burn-in will be out Thursday (Nov 18) and that Henrik will bring them with him to CERN on Monday (Nov 22).

Status of Designs:

AR2B: Production stuffing is starting today and the boards should ship in 1 to 2 weeks.

AR3F: There has been no communication with Bjorn in the past week. The last design that was received for these boards still had a few non-trivial noise issues and will need more work.

AR3B: ACAMAS is starting to work on the stuffing kit. They were sent 4 panels and parts for 36 panels.

AR2F: Nothing has changed. Still expecting boards at the end of November.

Prep for AR2B testing:

Bjorn can come help in theory as long as the AR3F design is finished in the next two weeks, but that is up in the air as always. Other things that will be going on at the same time are AR3B pre-series and possibly an AR2F pre-series before Christmas. There will be about 2 weeks before the Christmas shut-down to do work on the AR2B boards.

Low voltage offsets in the test-beam:

There had been a string of emails sent around concerning the inconsistent offsets between the analog and digital ground planes on the AR boards in the test beam. This is almost certainly being caused by imperfect load matching somewhere in the digital LV power supply system, but the exact source is unknown. There was some question as to whether poor crimps in the molex low voltage connector could be causing this. Ben reported that he went to the test beam area and measured the drops across the connector for the digital return lines on a few of the boards with the worst offsets. This was done by using an exact-o-knife to cut away the insulation on the wire just before and just after the connector and the potential drop was measured. In each of three cases, the potential drop was seen to be 5mV. Given that the current that is expected to be flowing through these lines is roughly 1 amp, this means that the crimps are making approximately a 5milliohm connection, which was taken to be fairly good. The offsets, some of which are on the order of 60mV, are most likely not being affected by this.

Miscellaneous issues:

PENN reports that 6 more boards have been repaired and that there could be 6 more by the end of the day. These boards will be shipped to NBI right away.

Harold asks if a spreadsheet can be created that lists the current location of each board (i.e. CERN, PENN, NBI).

Rick notes that no progress has been made on creating a re-work database. With the current procedure we will know which boards were repaired in which way, but the tests that are done along the way are not stored. Fido says that we need to enact a better plan for the type 2 boards. He suggests some sort of traveler that tracks where the board has been and what has been done to it along the way.