Minutes of the June 29, 2004 TRT Barrel Electronics Meeting
(Action items on Red)

1. Status of type 1 Production Boards

Rick: ACAMAS made a mistake, and for the filter capacitors on the threshold lines, 10 nF capacitors were stuffed instead of the 100 nF requested. ACAMAS has offered to replace them (it was their fault), but will imply days, perhaps weeks of delay. At Penn Anton has made tests with 10 nF and 100 nF and sees no difference. This is holding the order of the whole module type 1 production boards (28~33 boards of each type). Rick proposes to go ahead with the 10 nF after hearing Mitch opinion, that should be sometime today. Go ahead with such proposal

2) SR-1 Module Installation. Discussion of Interlock Systems.

Discussion of Interlock Systems:

Ricks points out two scenarios: 6 module tests (one sector) for which cooling and interlock is mandatory, and two module test, for which cooling and interlock is somewhat open to discussion (fans can be used). John replies, that using the cooling even for the two modules will be more practical, therefore software interlock through DCS could be used (as implemented right now in the test beam). Rick suggests some kind of hardware alarm using a thermistor and a boozer. It should be easy to implement for the test beam setup. John points out that for the installation maybe better to lock the interlock not to the on-board temperature but to the flow of cooling.

Regarding the on-board temperature, Fido points out that a decision must be taking about what patch panels has to be used on the integration (with the new patch panels, on-board temperature sensors are routed together with the harnesses, and a connector on the TTC is provided. End-Cap patch panels have no such provision). However, the new TTC patch panel pin-out connector seems to be incompatible with the final harnesses (that is what we want to use). Brig: a phone conference should be set-up with all the people interested on the patch panels present. An agreement on the pin-out should be made. New modified test patch panels should be produced, in order to be able to use the final harnesses. A phone meeting will be held on Friday 16.00.

3) Update on Test Beam Performance.

Mike and Toni show a table with the number of boards/chips working. All the DTMROCs on all the boards are functional. For the ASDBLR, the 2BL1 is completely missing, the 3BL1 is missing as well after the cooling incident (no electronics cooling for 24 hours, cooling plate temperature 90 C) and in some other positions 4 chips are missing now (not before the cooling incident). During tomorrow access Carl will try to fix 2BL1 (together with the other non responding chips) checking the cables. In addition, for the 2BL1 the cables will be swap with the upper sector. 3BL1 will be investigated (most probably, ASDBLR power failure).

Mike and Toni also show noise performance of the chips after the cooling incident. No relevant changes.

4) Other businesses:

Anatoli: when we will have another 3BL boards.

Rick: a new board completed at Penn, should be sent out to CERN on Friday.

Harold: status on the adjustments on the type 3 Boards

Rick: Nandor discovered on Bjorn dessings a discrepancy on hole sizes, due to the fact that Bjorn was using outdated Curt drawings. In progress???

Harold: status of the type 2 boards

Rick: The type 2Bs are now at CERN and final. They have one 2FL at CERN. A 2FS at Penn, next on the Godwin's stuffing list. There is a problem about the size of one of the mechanical holes, but can be easily fixed asking the manufacture drilling the correct size.

Rick believes ready to set a PRR.
Fido: for PRR needs to be taken into account involved people vacation (e.g. Philippe goes out for 3 weeks. Philippe fins a replacement). Setup a PRR date is one of the follow-up items for the next meeting.

Harold: in SR-1 we have already four modules installed, and soon (Friday) will be ready for electronics testing. Where we are in terms of infrastructure to test them?

All: Mike and Toni right now busy supporting test beam. Ben can help on SR-1. He sees no reasons not to have in 20 minutes the modules read-out operational.

5) Brief Update on System Performance at H-8

We read back all the type 1 boards of one sector. 2BL and 3BS still to be tested. Mitch is actively debugging the system (cold solder problems, shorted cables)