Minutes of the July 28, 2004 TRT Barrel Electronics Meeting
(Action items on Red)

1. Remaining items for Type 2 signoff (PENN)
Mitch updates his studies from the last week (http://www.hep.upenn.edu/atlas/PCBOARDS/Active_Roof_Boards/AR2_Boards/AR2FL_followup.ppt). He shows that the anomalous noisy channel observed in one chip was due to a bad placement of the board on the module. Once the board was plugged again on the module, the noisy chip disappeared.
He also has investigated low gain channels with an external charge injector. He confirms that observed low gain channels with the internal pulser have a gain at least 20 times lower than normal channels. These channels were not detected during the chip testing.

2) Update on status on SR-1 (Ole, Ben)
Condensation on the cooling system of the VME rack on SR-1 caused water to fall on the top of the rack power supplies, causing a short and damaging them.
Action: Ole is installing a new power supply. The temperature of the cooling system has been raised, so water condensation on the surface of the cooling system at the ambient temperature does not take place anymore.

3) Report on preliminary test results for type 1 boards (Penn)
Ben reports by mail:

This is a summary of the results from testing the full lot of type 1 boards here at CERN. I'll break it down by type because there seems to be a difference between types. There are also certain classes of failures, so I'll describe those first.

Shorts. These are primarily between the large ground pad at the end of the connector and the pin next to it. Sabetta is very good at fixing these, so they aren't that much of a problem.

No gain. These are channels where the noise case and the test pulse case both give the same 50% occupancy threshold. Such threshold is generally at about 55 DAQ counts (a "normal" channel has a noise response at about 70-80). When you probe the ASD input corresponding to these channels, you see a resistance that is lower than the nominal by about half, and when you power the board, you see an operating voltage that is higher than the nominal by about 50mV. If you were to look at a counting rate (edges) curve for one of these channels, you would see it is thinner than what it should be.

Dead chips: either an ASDBLR or a DTMROC that is not doing what it is supposed to. This is inferred from 8 or 16 consecutive channels reading back as always zero edges.

Low power resistance: a few boards had very low resistances (when not powered) in the power circuit that, while maybe not a cause of problems in itself, were correlated to boards with serious read-out problems.

Offsets: I'm not listing these below, but be aware that there are many of these (generally a few per board), mostly to the lower side and on the order of 10-20 DAQ counts, though there are some that are as much as 40 or 50 DAQ counts below the nominal. There are also a few offsets that are positive-going.

Perfect boards: all channels working, no large offsets.

AR1BS
Total boards tested: 12
Perfect boards: 6
No gain channels: 3

Comments: so far there are no serious problems with the boards that have been tested.

AR1FL
Total boards tested: 28
Perfect boards: 8
No gain channels: 24
Connector shorts: 5
Dead chips: DTM: 1
ASD: 1
Low power resistance: 1 (~50 ohms instead of ~300 ohms nominal)

AR1FS
Total boards tested: 28
Boards successfully read out: 24
Perfect boards: 3
No gain channels: 20
Connector shorts: 2
Dead chips: DTM: 1
ASD: 1
Low power resistance: 2 (50 instead of 300 and 50 instead of 500)

Comments: notice that it is only in the AR1FS boards that I've had trouble reading out. I haven't taken the time yet to look into this, so I don't really know what is causing this and why it is only showing up in these boards. There are a few chips in here that are either flaky or have strange gain, but I haven't listed them. Again, this will need to be looked into.

Other failures include either even or odd test pulse taking the wrong value (either not responding or too high, generally a stuffing error) and whole positions (16 channels) having a higher gain than normal. These were all seen in the 1F boards only.

4) Discussion of plans for testing/burn-in for type 1 boards (All)
Brig: in order to speed up the process, for the first batch we should do the all the testing at CERN, and send the boards to burn-in to NBI for a week.
All: it is enough a week?

Rick: two weeks was considered a very conservative election a long time ago. One week should be enough.

5) Discussion of criteria for acceptance of type 1 boards (All)

Ben reports:

Hi Everyone,
Now [..] we've got some statistics, […] For the record, when I say dead here I really mean channels that don't respond to an external stimulus. These are almost all from these "no gain" channels that we have been seeing.
Here are the numbers for AR1F (NOT integral): out of 43 boards with nothing worse than a few dead channels, there are this many boards with…
0 channels dead: 18.....
1 channel dead: 14.....
2 channels dead: 6.....
3 channels dead: 4....
4 channels dead: 1.

for the AR1B boards, we have:
out of 31 boards...
0 channels dead: 23.....
1 channel dead: 6.....
2 channels dead: 0
3 channels dead: 2..

There are other boards with whole chips out or other problems that will obviously require re-work, but for the others I just wanted to get a sense of which boards to hold out and which to send along. We can probably discuss this more in the meeting tomorrow anyways. It may also be worth noting that while a few of the 2 and 3 channel dead boards have all of those channels isolated on one ASDBLR, the one 4 channel dead board has those 4 channels spread across 4 different ASDBLRs.

Brig: we should not accept boards with more than one bad channel.
Rick: with the number of available ASDBLR chips, this constrain can be too tight. We must also decide how many chips do we want to replace.

Action: Ben to send to Penn for repair all the boards with problems or more than one bad channel.